Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices

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Abstract: The switching behavior of semiconductor devices responds to charge/discharge phenomenon of terminal capacitance in the device. The differential capacitance in a semiconductor device varies with the applied voltage in accordance with the depleted region thickness. This study develops a C-V characterization system for high-voltage power transistors (e.g., MOSFET, insulated gate bipolar transistor, and JFET), which realizes the selective measurement of a specified capacitance from among several capacitances integrated in one device. Three capacitances between terminals are evaluated to specify device characteristics-the capacitance for gate-source, gate-drain, and drain-source. The input, output, and reverse transfer capacitance are also evaluated to assess the switching behavior of the power transistor in the circuit. Thus, this paper discusses the five specifications of a C-V characterization system and its measurement results. Moreover, the developed C-V characterization system enables measurement of the transistor capacitances from its blocking condition to the conducting condition with a varying gate bias voltage. The measured C-V characteristics show intricate changes in the low-bias-voltage region, which reflect the device structure. The monotonic capacitance change in the high-voltage region is attributable to the expansion of the depletion region in the drift region. These results help to understand the dynamic behavior of high-power devices during switching operation.

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