System Design and Simulation of a HIPERLAN/2 Receiver Frout-End

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Abstract :

A simple method to model and simulate a Hiperlan/2 receiver front-end is presented. The heterodyne radio architecture is chosen to study due to its simplicity. For reference, the filter, the amplifier, and the mixer used in this linear system simulation have their parameters set to values that are commercially available. Simulations employed a commercial CAD are used to investigate the receiver performance by injecting one-tone RF carrier of 5.2 GHz. Required standard HIPERLAN/2 of maximum sensitivities at -68 dBm and minimum at -20 dBm are injected into the designed system. A harmonic balance analysis is used to perform both frequency and time domains of the receiver. Verification in the frequency and time domains shows that the system is capable of detecting the IF 280 MHz at the same levels as designed in the power link budget under linear simulation environment. This means that a more complex circuit-level may be further implemented when standard test signals are added.

Keywords : WLAN, HIPERLAND/2, radio receiver.

1. Introduction

Wireless engineers nowadays face tremendous pressures in designing compact, cost - effective, and low-power consumption transceivers. These include wireless standards such as Bluetooth, IEEE 802.11a, and HIPERLAN/2, which normally employ sophisticated digital modulation formats to achieve the required data rate over noisy communi cation channels. Especially in radio design section, engineers must carefully consider their radio architectures not only to achieve above requirements but also the feasibility to implement those designs into standard specifications.

For example, a 2.4 GHz Bluetooth standard design and implementation of a transceiver front-end using a heterodyne architecture has been demonstrated [1]. It is concern with circuit designs of each functional block including a low noise amplifier (LNA), an oscillator, and a mixer. Having designed and characterization, all circuits are connected together where sample data is injected to investigate the overall performance.

This paper, however, presents an alternative approach for a transceiver design. A system-level design is considered to be a case study, which illustrates the importance of simulating RF designs for the required specifications. It would be shown that such a system-level design plays an important role not only for system but also circuit engineers who would like to verify the overall system performance before considering a line production

Initially, a system-level design is verified with a commercial CAD of Agilent's Advanced design

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System (ADS). The ADS is used to evaluate the system performance by means of one-tone RF input 5.2 GHz. The standard RF parameters used in this work are based on the European HIPERLAND/2 radio specifications [2]. Due to a short period of time for characterization, further work on a circuit-level implementation will be made to demonstrate and compare with the current simulated results.

2. System review

According to the HIPERLAN/2 radio require ments, the receiver must be able to provide data rate up to 54 Mbps in which its channel bandwidth is limited to 20 MHz. The minimum receiver sensitivity is -68 dBm and the maximum is -20 dBm. The lower frequency band (for indoor purposes) is assigned between 5.15 GHz to 5.35 GHz. However, a single tone RF input of 5.2 GHz is used in this work.

The proposed radio receiver front-end is a heterodyne architecture similar to [1]. The heterodyne receiver is chosen because of its structural simplicity when compared to other architectures such direction conversion, low IF, or wideband IF double conversion architectures. The receiver block consists of an LNA, a mixer, an oscillator, and an IF filter as shown in Figure 1.

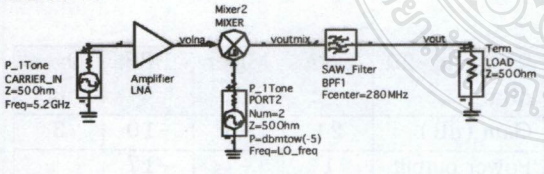

Figure 1 Receiver block diagram.

At the input of the receiver, the RF carrier of 5.2 GHz is fed into the LNA by an arbitrary waveform from a function generator. Then, the amplified signal is downconverted to the IF of 280 MHz. Finally, the bandpass filter is used to pass the desired signal for further processing (which is out of scope of this work).

3. Receiver design

A number of parameters are needed to perform. Firstly, the receiver noise floor. The noise floor is used to describe input noise power that appeared at the receiver input, given by [3]:

$$\text{Noise floor} = kTB \quad (1)$$

where k is the Boltzman's constant (1.38×10^{-23}), T is the temperature (290 K), and B is the channel bandwidth. From Equation (1), the noise floor is found to be -101 dBm.

For sending data at the rate of 54 Mbps, the carrier-to-noise ratio (CNR) of 20 dB is needed, which produces 1% bit error rate [4]. Having CNR, the maximum allowable noise figure (NF) (per Hertz) of the receiver can be computed from Eq. (1). The calculated NF is 13 dB.

$$\text{NF} = \text{sensitivity} - \text{CNR} - \text{noise floor} \quad (2)$$

Having obtained noise figure of the receiver, the minimum detectable signal (MDS) can be calculated. MDS is defined as the ability of the receiver to detect signals above the noise floor. The MDS equation calculates a signal power at the input, which takes into account noise added by system [3]. The MSD is found to be -88 dBm calculated from Eq. (3).

$$\text{MDS} = \text{noise floor} + \text{NF} \quad (3)$$

4. Link budget analysis

The RFIC chipsets shown in Figure 1 consist of the AR7541A 5-6 GHz LNA [4], the HMC 218MS8 double-balanced mixer [5], and the TQS-444F-TR surface-acoustic wave filter [6]. Summaries of the power link budget using the RFICs are shown in Table 1 and 2 for the sensitivities of -68 dBm and -20 dBm, respectively.

It has been previously shown that the estimated system NF is 13 dB while the designed receiver NF from the tables is only 4 dB. This should be sufficient since the LNA is usually connected to a duplexer that has its loss of around 3 dB. Besides, if another implementation loss is included e.g. 3 dB, the total NF would be 10 dB. This means the total NF is still less than its maximum allowance.

5. Simulation results

Simulations are set up for two input levels i.e. -68 dBm and -20 dBm. Parameters of each functional block are added such as gain, noise figure, s-parameters, etc. as specified in the manufacturers' data sheets. The results obtained when -68 dBm is added are shown in Figure 1 to 3. Signals in Figure 1 show the input of 5.2 GHz and output of 280 MHz. It can be seen that the output power is close to the estimated value shown in Fig. 1. Fig. 2 shows waveforms at the input and at the output of the mixer. At this stage, signals from the mixer are not only the desired IF but also undesired mixing products. When the BPF is added into the system, those products are filtered out where the desired IF passes through with attenuation. Fig. 3 shows the IF waveform (compared to the waveform before BPF) where its spectrum is shown in Fig. 1.

Fig. 4 through Fig. 5 show input and output signals when the carrier level is set to -20 dBm. Obviously, the signals are exactly the same as the previous 3 Figures except the increased power levels. It can also be seen that the receiver front-end is capable of producing the desired IF signal at the level which is exactly the same as estimated in Table 2.

6. Conclusion

A simple method to model and simulate a European HIPERLAN/2 receiver front-end using RFICs is presented. The results from simulations at low-end and high0end sensitivities have been shown that the receiver is capable of detecting the desired incoming signals. Interestingly, It should be noted that this system simulation is not an experimental approach, in which many practical issues are not yet considered such as real-time signal, non-linearity, and etc.

However, this work intently shows that system-level design is a very useful method for system engineers who need to use the available products and the commercial CAD to verify their designs. After system verification, a complexity in developing a prototype can be reduced.

In the future, a full system implementation will be carried out where standard HIPERLAN/2 data will injected instead of one-tone technique as presented here.

RF input -68 dBm	LNA	Mixer	BPF	Over all
Gain (dB)	21	-8	-10	3
Power output (dBm)	-47	-55	-65	
Noise figure(dB)	3.5	8	10	4

Table 1 Link budget with -68 dBm sensitivity.

RF input -20 dBm	LNA	Mixer	BPF	Over all
Gain (dB)	21	-8	-10	3
Power output (dBm)	1	-7	-17	
Noise figure (dB)	3.5	8	10	4

Table 2 Link budget with -20 dBm sensitivity.

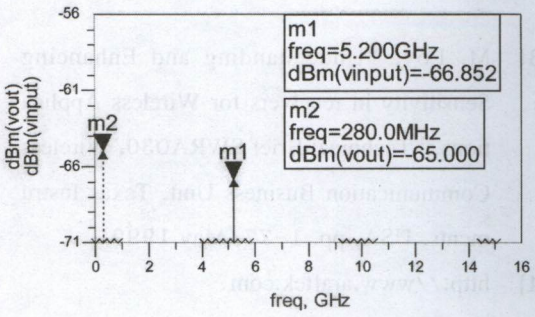

Figure 1 Spectrum of the input and output signals.

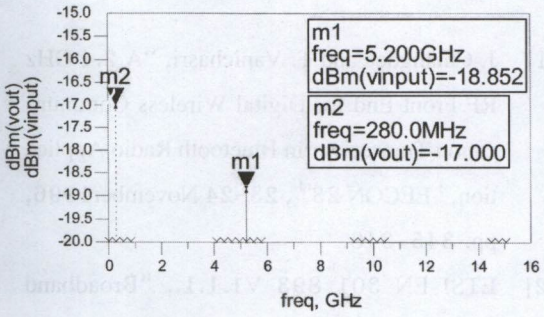

Figure 4 Spectrum of the signals.

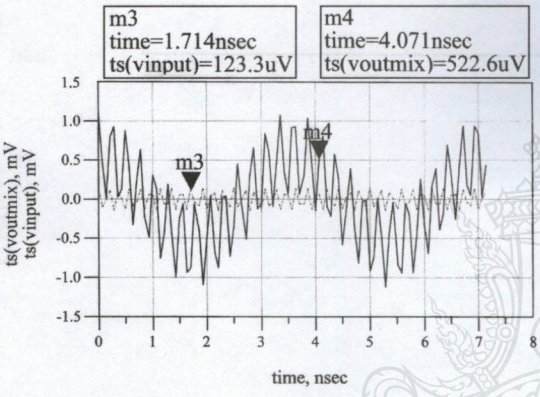

Figure 2 Waveforms at the input port and the mixer output port.

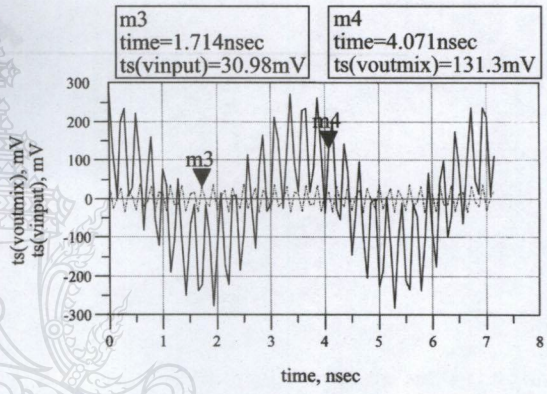

Figure 5 Waveforms at the input port and the mixer output port.

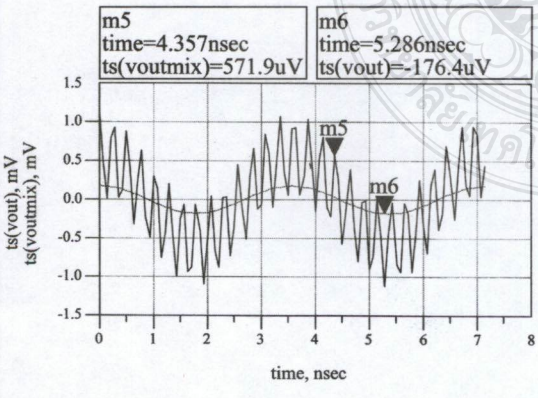

Figure 3 Waveforms at the mixer output port and the desired IF.

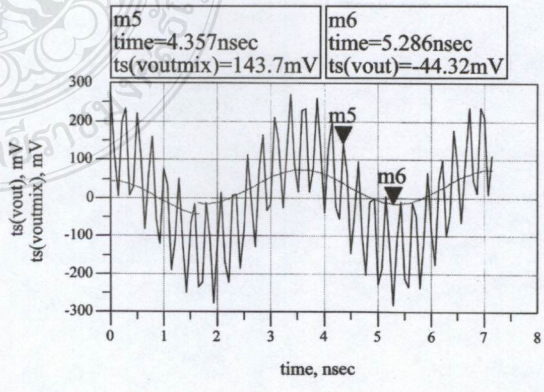

Figure 6 Waveforms at the mixer output port and the desired IF.

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