Multilevel Topologies-Prototype : Description and Modeling

Paisan Boonchiam*

Abstract

Multilevel Topologies are studied in this paper. These static converter can generate three or more levels in each output phase, and are generally applied to high-power applications because of their ability to operate with larger voltages than the classical two-level converter. The analysis is mainly focused on the three-level topology, although there are also some contributions for converters with a larger number of levels. The main objectives are to show the prototype and modeling of multilevel converter.

Index Terms – Multilevel Converter, Modeling and Control.

1. INTRODUCTION

In recent year, there has been a growing interest in power electronics systems. One reason for this is the increasing utilization of electric and electronic equipment, not only for industrial in improving the efficiency of systems, besides the expansion of the application of renewable energies. This growing demand has favored the development of new power electronics devices, as well as novel power converter topologies.

For high power applications, voltage and current must be pushed up. Hence, maximum rating of power semiconductors become a real handicap. Paralleling devices, subsystems or systems leads to higher current levels. On the other hand, series connections are the solution for dealing with larger voltages. Nevertheless, given a chain of devices connected in series, achieving static and dynamic voltages applied to the devices is clamping those using DC voltage source; or large capacitors, which transitorily behave as voltage source. Multilevel topologies are based on this principle,and therefore, the voltage applied to the devices can be controlled and limited. An advantage of multilevel converters compared with the classical two-level topology, is that the output voltage spectra are significantly improved due to having a greater availability of voltage levels. Hence, the output voltage can be filtered with smaller reactive components, and additionally, the switching frequencies of the devices can be reduced. These two benefits, together with the ability to deal with high voltage levels, confer on multilevel converters a very important role in the field of high power applications.

This paper shows an extended introduction that describes and discusses the main multilevel converter topologies. At the same time, it describes the prototype used for the experimental results presented in this paper, which is a part of energy system. In addition, the diode-clamped multilevel converters are modeled so that commutated and average models can be used for simulations. An averaged small-signal model of the three-phase converter is described for the design of control loops.

2. MULTILEVEL TOPOLOGIES

There is growing interest in multilevel since they can extend the application of power electronics systems to higher voltage and power ratios. Multilevel converters are the most attractive technology for the medium- to high-voltage range (2-60 kV), which includes motor drives, power distribution, power quality and power conditioning applications.

Multilevel converters can synthesize waveform by using more than two voltage levels; hence, the quality of the spectra is significantly improved compared with the classic two-level topology. The main drawbacks of the multilevel converters are that:

* Department of Electrical Engineering, Faculty of Engineering, Rajamangala University of Technology Thanyaburi, Pathumthani, Thailand 12110
E-mail: paisan.b@en.rmutt.ac.th

⇨ These topologies require a high number of switches,

⇨ Their control is difficult because of such amount of devices, and

⇨ Several DC voltage source are required, which are usually provided by capacitors. Balancing the voltage of these capacitors according to an operating point is a difficult challenge.

Despite these drawback, multilevel converters have turned out to be a very good alternative for high-power applications, since the cost of the control for these cases is a small portion of the whole cost of the system. Furthermore, as prices of power semiconductors and DSPs continue to decrease, the use of multilevel topologies is expected to extend to low-power applications as well. Fast power devices, which can operate at very high switching frequencies, can be used for low voltages. Therefore, the values of the reactive components will undergo significant reduction. Furthermore, new power devices are expected to appear in the next some years, and these may also extend the application of multilevel topologies.

So far, the most actively developed multilevel topologies are:

⇨ The diode-clamped converter,

⇨ The floating-capacitor converter, and

⇨ The cascaded H-bridge converter.

Other name are used to define these topologies. For example, when referring to the three-level diode-clamped converter, it is also called the NPC converter. This name cannot be extended to topologies with a higher number of levels because of the multi-clamped point available. These systems can operate as inverter or as rectifiers, depending on whether the energy flux flows from the DC to the AC side, or from the AC to the DC side, respectively.

2.1 Diode-clamped Converter

Since its introduction in 1981 by Nabae et al [1], this three-level diode-clamped converter has been the most practical and widely studied multilevel topology. For the general case of an n-level topology, n-1 consecutive switches of each leg must be in the on-state. As a result, a defined voltage level of the series capacitors is connected to the output. Three single-pole n-throw switched, as show in Fig. 1, can perform as functional diagram of this converter.

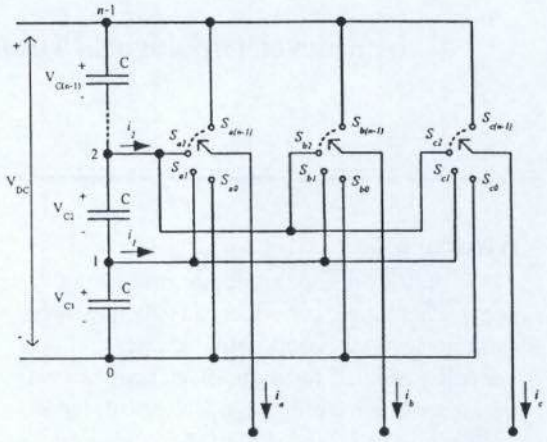

Fig. 1: Functional diagram of the n-level diode-clamped converter.

Expression (1) summarizes all of the possible combinations. The variables s_{ij} are the control functions of the single-pole n-throw switches. These variables define the position of the switches, so that they have the unity value when the i output is connected to the j point; otherwise they are zero (s_{ij}={0,1}).

$$\sum_{j=0}^{n-1} s_{ij} = 1 \qquad \text{with i=\{a, b, c\}} \qquad (1)$$

Referring all of the voltage to the lower DC-link voltage level ("0 reference), each output consists of contributions by a determinate number of consecutive capacitors:

$$v_{i0} = \sum_{j=1}^{n-1} \left(s_{ij} \sum_{p=1}^{j} V_{Cp} \right) \text{ with i=\{a, b, c\}} \quad (2)$$

When balanced distribution of the DC-link voltage among the capacitors is assumed:

$$v_{i0} = \frac{V_{DC}}{n-1} \sum_{j=1}^{n-1} j \, s_{ij} \qquad \text{with i=\{a, b, c\}} \quad (3)$$

Under balanced conditions, the maximum forward voltage applied to the switches of the bridge is the voltage of one single capacitor.

The advantages of the diode-clamped converter compared with other multilevel topologies are that:

⇨ They use a low number of capacitors. Although these topologies require some additional

clamping diodes, their low number of reactive components is usually preferred from the standpoint of cost.

⇨ They can be connected to a single DC-link voltage. The floating-capacitor topology also shares this advantage, but the cascade converter does not, since this converter requires multiple isolated DC power supplies.

Nevertheless, some practical experience with this topology reveals technical difficulties that complicate its application, as follows:

⇨ For topologies with more than three levels, the clamping diodes are subject to high voltage stress equal to $V_{DC}(n-2)/(n-1)$. As a result, series connection of the diodes is required. The issue complicates the design and raises reliability and cost concerns.

⇨ The objective of maintaining the charge balance of the capacitors in topologies with a high number of levels has been demonstrate to be impossible for some operating conditions. These balancing problem appear when dealing with deep modulation indices and active currents. Therefore, high AC output voltages cannot be achieved, which inhibits the most important attribute of multilevel converters. Significant balancing improvements are obtained when two or more converters are connected to the same DC link. These converters are also used for static VAR compensation circuits in which no active power is transmitted and the balancing problem can be handled.

⇨ Although proper control of the three-level topology overcomes the voltage balance concern, a low-frequency ripple in the NP potential appears when dealing with large modulation indices and low PFs. The maximum voltage applied to the devices is higher due to this oscillation, and additionally, it produces low-frequency distortion in the AC output voltages. Some solutions for this problem are proposed in this paper.

2.2 Floating-Capacitor Converter

Meynard et al. [1, 2] introduced the floating -capacitor converter. In this topology the voltage clamping is achieved by means of capacitors that "float" with respect to the earth potential.

Each leg of these topologies can be seen as an imbricate cell where the output voltage is synthesized by connecting a defined number of capacitors in series.

One out of each pair of switches s_{Hi} and s_{Li} must be in the on-state for a proper connection to exist between the DC-link potential and the output through some capacitors. Additionally, both switches cannot be on at the same time or else short circuits will occur in the capacitors.

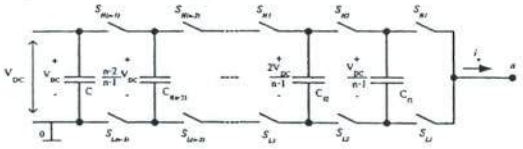

Fig. 2: Imbricate cell, base of the floating-capacitor converter.

Some important conclusions related to the voltage balancing issue in the floating-capacitor converters are as follows:

⇨ Each leg can be analyzed independently from the others. This is an important difference with the diode-clamped converter, in which the entire three-phase system must be considered for the balancing issue.

⇨ These converters can control the voltages of the floating capacitors tanks to their redundancy of states. However, in converters with more than three levels, some transitions between two consecutive voltage levels produce high switching frequencies. If these transitions are avoided, the amplitude of the voltage ripple in the capacitors will increase, and it might not be controllable.

In conclusion, one of the major drawback of this topology is its high number of capacitors, not only those in the topology itself, but also those required for the series and parallel connections.

2.3 Cascaded H-bridge Converter

One of the earliest applications for the series connection of single-phase full-bridge inverter topology was its use for plasma stabilization in 1988 [4]. Later, this approach was extended to include three-phase systems.

The modularity of this topology is an important feature. However, the fact that the DC-link voltage must be isolated is the major drawback for application of these structures. Several independent DC power supplies are required, which

can be provided either by a transformer with multiple isolated secondaries or by several transformers. For electrical vehicles, batteries or fuel cells can also be used.

In order to balance the power provided by the DC voltage source, each cell can be used in a cyclic way throughout each semi-cycle of a line period [5]. Another benefit of this circulating method is that it achieves the same switching frequencies for all of the devices.

For a given topology, a higher number of levels can be obtained of each cascade level is fed by a different DC voltage value. Different devices would make up each cell, so that the fastest ones, which may synthesize the cell fed by the low voltage, will define the output voltage switching frequency [6].

3. MODEL OF DIODE-CLAMPED CONVERTER

Some model of the diode-clamped converter are presented in this section. General models are given for multilevel topologies (n-level), and they are also particularized for the three-level case.

Different kinds of models are required:

⇨ "Large-signal" models. These mathematical models are used to obtain simulated results for the converter. They are formulated in terms of control functions of the switches. Nevertheless, if the switching functions are substituted by their duty cycles, the waveform obtained are free of certain components related to switching frequency. These models may be interesting in terms of ability to analyze transitory average evolutions of voltages and currents, as well as to perform low-frequency analysis.

⇨ "Small-signal" model. This model is required to design and study control loop strategies. As the control stage must achieve the operation point of the system while disregarding high-frequency components of the variables (switching frequency), this model is formulated in terms of local average variable. State-space formulation is used for the model.

3.1 Multilevel Models

Fig. 3 shows the diagram of multilevel system to be modeled. Conventional signs of voltage and currents are also indicated.

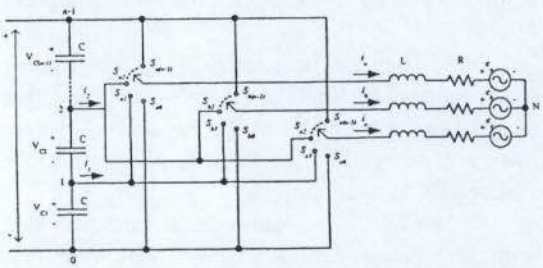

Fig.3: General multilevel system to be modeled.

3.2 Phase Model

The output voltage in Fig. 3 referring to the lower DC-link potential ("0") can be expressed as:

$$v_{i0} = L\frac{di_i}{dt} + Ri_i + e_i + v_{N0} \qquad (4a)$$

where i={a, b, c}.

The AC NP potential ("N") can be found by summing all the terms in (4), and in regards to the fact that $i_a + i_b + i_c = 0$, then:

$$v_{N0} = \frac{v_{a0} + v_{b0} + v_{c0} - (e_a + e_b + e_c)}{3} \qquad (5)$$

A first-order matrix equation describes the AC side of the system, such that

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{v}_{ph0} - \frac{1}{L}\mathbf{U}_3 v_{N0} \qquad (6)$$

where the subscript *ph* indicates the following phase components:

$$\mathbf{i}_{ph} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad \mathbf{e}_{ph} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}, \text{ and } \quad \mathbf{v}_{ph0} = \begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix}$$

The tern $\mathbf{U}_3$ in (6) is a conventional notation that stands for $[1\ 1\ 1]^T$.

On the other hand, the following equation indicates the currents through the capacitors in the DC side of the converter:

$$i_{Cj} = C\frac{dv_{ci}}{dt} = i_{DC} - \sum_{k=j}^{n-1} i_k \quad \text{where j=\{1,2, .., n-1\}} \quad (7)$$

Or

$$\frac{d}{dt}\mathbf{v}_c = \frac{1}{C}\mathbf{U}_{n-1} i_{DC} - \frac{1}{C}\mathbf{K}_{NC}\mathbf{i}_{NC} \quad (8)$$

where

$$\mathbf{v}_c = \begin{bmatrix} v_{c(n-1)} \\ v_{c(n-2)} \\ \vdots \\ v_{c2} \\ v_{c1} \end{bmatrix}, \quad \mathbf{i}_c = \begin{bmatrix} i_{(n-1)} \\ i_{(n-2)} \\ \vdots \\ i_2 \\ i_1 \end{bmatrix}, \text{ and}$$

$$K_{NC} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ 1 & 1 & \cdots & 1 & 0 \\ 1 & 1 & \cdots & 1 & 1 \end{bmatrix}$$

Equation (6) and (8) describe the entire system expect for the switching stage. The control functions of each single-pole n-throw switch can interrelate voltages and currents between the AC side and the DC side of the converter, such that

$$\mathbf{v}_{ph0} = \mathbf{s}_{ph}\mathbf{v}_C; \quad \mathbf{K}_{NC}\mathbf{i}_{NC} = \mathbf{s}_{ph}^T\mathbf{i}_{ph} \quad (9)$$

where the switching matrix is:

$$\mathbf{s}_{ph} = \begin{bmatrix} s_{a(n-1)} & s_{a(n-1)} + s_{a(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{ai} & \sum_{i=1}^{n-1} s_{ai} \\ s_{b(n-1)} & s_{b(n-1)} + s_{b(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{bi} & \sum_{i=2}^{n-1} s_{bi} \\ s_{c(n-1)} & s_{c(n-1)} + s_{c(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{ci} & \sum_{i=2}^{n-1} s_{ci} \end{bmatrix}$$

By substituting (9) into (6) and (8), a set of dynamic equations describing the switched model of the multilevel system is developed. This model is general, complete and makes no assumptions other than the use of ideal switched:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph}\mathbf{v}_C - \frac{1}{L}\mathbf{v}_{N0} \quad (10a)$$

$$\frac{d}{dt}\mathbf{v}_c = \frac{1}{C}\mathbf{U}_{n-1}\mathbf{i}_{DC} - \frac{1}{C}\mathbf{s}_{ph}^T\mathbf{i}_{ph} \quad (10b)$$

Although this mathematical model can be used for simulations, the term v_{N0} must be calculated during the simulation, which involves solving for voltage v_{a0}, v_{b0} and v_{c0}. However, if the system equation is translated into dq rotating-coordinate frames, this term no longer affects any current because it is only involved in the homopolar current equation, which is always zero. As the voltage-balancing process of the capacitors will be performed by the modulation itself, the voltage v_{N0} does not provide any useful information for control. This term can also be achieved if the converter is modeled from the standpoint of line-to-line components.

3.3 Line-to-Line Model

To deal with line-to-line components, the terms of the consecutive equations in (4) are subtracted from each other, so that:

$$v_{ab} = L\frac{di_{ab}}{dt} + Ri_{ab} + e_{ab} \quad (11a)$$

$$v_{bc} = L\frac{di_{bc}}{dt} + Ri_{bc} + e_{bc} \quad (11b)$$

$$v_{ca} = L\frac{di_{ca}}{dt} + Ri_{ca} + e_{ca} \quad (11c)$$

where $v_{ab}=v_{a0}-v_{b0}$, $i_{ab}=i_a-i_b$, $e_{ab}=e_a-e_b$, etc.

Note that the AC NP voltage term has disappeared from these expressions.

By processing in a way similar to that for the phase model, the final equations of the line-to-line model are:

$$\frac{d}{dt}i_{LL} = -\frac{R}{L}i_{LL} - \frac{1}{L}e_{LL} + \frac{1}{L}s_{LL}v_C \quad \text{and (12a)}$$

$$\frac{d}{dt}v_C = \frac{1}{C}U_{n-1}i_{DC} - \frac{1}{3C}s_{LL}^T i_{LL} \qquad (12b)$$

where

$$\mathbf{i}_{LL} = \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} \text{ and } \mathbf{e}_{LL} = \begin{bmatrix} e_{ab} \\ e_{bc} \\ e_{ca} \end{bmatrix},$$

and where the switching matrix is:

$$\mathbf{s}_{LL} = \begin{bmatrix} s_{ab(n-1)} & s_{ab(n-1)} + s_{ab(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{abi} & \sum_{i=1}^{n-1} s_{abi} \\ s_{bc(n-1)} & s_{bc(n-1)} + s_{bc(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{bci} & \sum_{i=2}^{n-1} s_{bci} \\ s_{ca(n-1)} & s_{ca(n-1)} + s_{ca(n-2)} & \cdots & \sum_{i=2}^{n-1} s_{cai} & \sum_{i=2}^{n-1} s_{cai} \end{bmatrix}$$

with $s_{ijk}=s_{ik}-s_{jk}$; i, j ={a, b, c}; and k={1,2,…,n-1}.

The number three in (12b) appears because

$$i_p = \frac{1}{3}\left(s_{abp}i_{ab} + s_{bcp}i_{bc} + s_{cap}i_{ca}\right) \text{ with}$$

p={1,2,…,n-1} (13)

which can be demonstrated from

$$i_p = s_{ap}i_a + s_{bp}i_b + s_{cp}i_c \text{ and } i_a + i_b + i_c = 0. \qquad (14)$$

4. EXAMPLE OF THREE-LEVEL MODELS

Fig. 4 shows the diagram of the three-level system that has been modeled. Conventional signs of voltages and currents are also indicated.

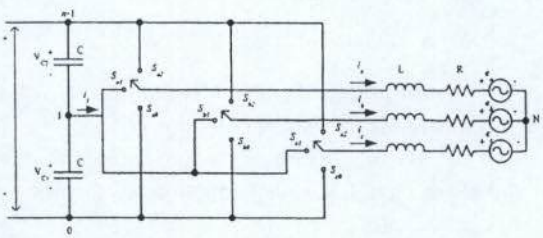

Fig.4: Conventional signs of the variables of the three-level converter.

4.1 Phase Model

The general equations (10a) and (10b) of the phase model are now applied to n=3 (three-level), such that

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3L}\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3\mathbf{v}_{N0} \qquad (15a)$$

$$\frac{d}{dt}\mathbf{v}_{C3L} = \frac{1}{C}\mathbf{U}_2\mathbf{i}_{DC} - \frac{1}{C}\mathbf{s}_{ph3L}^T\mathbf{i}_{ph} \qquad (15b)$$

where, for this particular case:

$$v_{C3L} = \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} \text{ and } {}^{s}{}_{ph3L} = \begin{bmatrix} s_{a2} & s_{a2} + s_{a1} \\ s_{b2} & s_{b2} + s_{b1} \\ s_{c2} & s_{c2} + s_{c1} \end{bmatrix}.$$

Since each single-pole three-throw switch only can take one position at any time, the switching matrix can be expressed as:

$$s_{ph3L} = \begin{bmatrix} s_{a2} & 1 - s_{a0} \\ s_{b2} & 1 - s_{b0} \\ s_{c2} & 1 - s_{c0} \end{bmatrix} \qquad (16)$$

By substituting this switching matrix into (16):

$$\mathbf{s}_{ph3L}\mathbf{v}_{C3L} = \begin{bmatrix} s_{a2} - s_{a0} \\ s_{a2} - s_{a0} \\ s_{a2} - s_{a0} \end{bmatrix}\begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} + \mathbf{U}_2 v_{C1} \qquad (17a)$$

$$\mathbf{s}_{ph3L}^T\mathbf{i}_{ph} = \begin{bmatrix} s_{a2} & s_{b2} & s_{c2} \\ -s_{a0} & -s_{b0} & -s_{c0} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (17b)$$

where, the equations of the three-level converter are:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3L}\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3\left(\mathbf{v}_{N0} - \mathbf{v}_{C1}\right) \qquad (18a)$$

$$\frac{d}{dt}\mathbf{v}_{C3L} = \frac{1}{C}\mathbf{U}_2\mathbf{i}_{DC} - \frac{1}{C}\mathbf{s}_{ph3L}^T\mathbf{i}_{ph} \qquad (18b)$$

where the new switching matrix is:

Referring the AC NP potential ("N") with the NP of the DC-link ("1"), (18a) becomes:

$$\frac{d}{dt}\mathbf{i}_{ph} = -\frac{R}{L}\mathbf{i}_{ph} - \frac{1}{L}\mathbf{e}_{ph} + \frac{1}{L}\mathbf{s}_{ph3L}\mathbf{v}_{C3L} - \frac{1}{L}\mathbf{U}_3 v_{N1} \quad (19)$$

4.2 Line-to-Line Model

The general equations of the line-to-line model are applied now to the three-level converter:

$$\frac{d}{dt}i_{LL} = -\frac{R}{L}i_{LL} - \frac{1}{L}e_{LL} + \frac{1}{L}s_{LL3L}v_{C3L} \quad \text{and} \quad (20a)$$

$$\frac{d}{dt}v_{C3L} = \frac{1}{C}U_2 i_{DC} - \frac{1}{3C}s_{LL3L}^T i_{LL} \quad (20b)$$

where, for this particular case:

$$v_{C3L} = \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} \text{and } s_{LL3L} = \begin{bmatrix} s_{ab2} & s_{ab2} + s_{ab1} \\ s_{bc2} & s_{bc2} + s_{bc1} \\ s_{ca2} & s_{ca2} + s_{ca1} \end{bmatrix} \quad (20c)$$

If the switching matrix is preferred to contain switching functions of the higher and lower connection poles ("2 and "0 subscripts), it can be expressed as:

$$\mathbf{s}_{LL3L} = \begin{bmatrix} s_{ab2} - s_{ab0} \\ s_{bc2} - s_{bc0} \\ s_{ca2} - s_{ca0} \end{bmatrix} \quad (21)$$

5. MODEL OF THE CONTROL

The small-signal model of the three-level converter is developed in this section so that proper control loops can be designed. This model is based on the phase model, but it could be based on the line-to-line model without significant differences.

5.1 State-Space Model

From (6):

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{L} \end{bmatrix}\begin{bmatrix} e_a - v_{a0} \\ e_b - v_{b0} \\ e_c - v_{c0} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} \\ -\frac{1}{L} \\ -\frac{1}{L} \end{bmatrix} v_{N0} \quad (22)$$

Transforming (22) into rotating frames according to the dq transformation:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ -\omega & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{L} \end{bmatrix}\begin{bmatrix} e_d - v_d \\ e_q - v_q \\ e_0 - v_0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -\frac{\sqrt{3}}{L} \end{bmatrix} v_{N0} \quad (23)$$

where ω is the line angular frequency. As the sum of the three line currents is zero, there is no homopolar component ($i_0 = 0$). Therefore, the AC NP voltage (vN0) does not affect any transformed current. This voltage can be deduced from (23) as:

$$v_{N0} = \frac{e_0 - v_0}{\sqrt{3}} \quad (24)$$

The AC NP voltage only depends on homopolar voltage components. Additionally, when the electrical grid is balanced, the average value of e_0 is zero; hence, v_{N0} depends only on the homopolar component of AC voltages of the converter.

Defining the original position of the dq axis to be e_q=0, the other component is e_d=EL, which is the value of the line-to-line RMS voltage. Therefore, (23) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix} E_L \quad (25)$$

where the homopolar component has been omitted.

On the other hand, from (8), the DC side of the system can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} = \frac{1}{C} i_{DC} - \frac{1}{C}\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} i_2 \\ i_1 \end{bmatrix} \quad (26)$$

In order to avoid switching functions, the equation of DC side (26) cab be related to AC side (25) by the power-balanced relationship. Taking into account that the dq transformation is power conservative:

$$p = v_a i_a + v_b i_b + v_c i_c = v_d i_d + v_q i_q \qquad (27)$$

and assuming efficiency of 100%, the instantaneous power at the DC side is:

$$p = (v_{C1} + v_{C2}) i_2 + v_{C1} i_1 \qquad (28)$$

Making both power values equal, current i_2 at:

$$i_2 = \frac{v_d i_d + v_q i_q - v_{C1} i_1}{v_{C1} + v_{C2}} \qquad (29)$$

and substituting this current into (26):

$$\frac{dv_{C2}}{dt} = \frac{i_{DC}}{C} - \frac{v_d i_d + v_q i_q - v_{C1} i_1}{v_{C1} + v_{C2}} \qquad (30a)$$

$$\frac{dv_{C1}}{dt} = \frac{i_{DC}}{C} - \frac{v_d i_d + v_q i_q - v_{C2} i_1}{v_{C1} + v_{C2}} \qquad (30b)$$

The large-signal model of the system in defined by (25) and (30).

Since the modulation algorithm will balance the NP voltage, the control stage must only regulate the total DC-link voltage and the AC currents. Therefore, the model can be simplified assuming balanced voltages in the capacitors ($v_{C1}=v_{C2}=v_{DC}/2$). Summing term by term in (30).

$$\frac{dv_{DC}}{dt} = 2\frac{i_{DC}}{C} - 2\frac{v_d i_d + v_q i_q}{C v_{DC}} \qquad (31)$$

This equation is nonlinear; therefore, it should be linearized to obtain a useful model for the control. Average variables are assumed, according to the local averaging operator:

$$\bar{x}(t) = \frac{1}{T_m} \int_{t-T_m}^{t} x(\tau) d\tau \qquad (32)$$

As a result of applying this linear operator to the model of the system, all components of the variables related to switching frequency disappear. The variables of the model are assumed henceforth to be average variables. For the purpose of simplicity, no difference in notation has been included.

The variables assumed to be controlled are the reactive current component and the DC-link voltage:

$$i_q = i_q^* \quad \text{and} \quad v_{DC} = v_{DC}^* \qquad (33)$$

where i_q^* and v_{DC}^* denote the reference values.

The transformed AC voltages of the converter (v_d, v_q) are the control variables. Thus, the system is simplified to two-input-two-output three-order system.

In steady-state conditions, the subscript "ss" is added to the variables to identify the operating point:

$$e_{dss} = E_L,\ e_{qss} = 0,\ i_{qss} = i_q^* \text{ and } v_{Css} = v_{DC}^* \qquad (34)$$

The remaining steady-state variables are found by imposing zero into the dynamic of the system; in other words, they are obtained by making the derivatives of variables equal zero, as follows:

$$\frac{di_{dss}}{dt} = -\frac{R}{L} i_{dss} + \omega i_q^* + \frac{1}{L} v_{dss} - \frac{1}{L} E_L = 0 \qquad (35a)$$

$$\frac{di_{qss}}{dt} = -\omega i_{ss} - \frac{R}{L} i_q^* + \frac{1}{L} v_{dss} = 0 \qquad (35b)$$

$$\frac{dv_{DCss}}{dt} = 2\frac{i_{DCss}}{C} - 2\frac{v_{dss} i_{dss} + v_{qss} i_q^*}{C V_{DC}^*} = 0 \qquad (35c)$$

Solving for the steady-state values:

$$i_{dss} = \sqrt{\left(\frac{E_L}{2R}\right)^2 + \frac{V_{DC}^*}{R} i_{DCss} - i_q^{*2}} - \frac{E_L}{2R} \qquad (36a)$$

$$v_{dss} = E_L + R i_{dss} - \omega L i_q^* \qquad (36b)$$

$$v_{qss} = \omega L i_{dss} + R i_q^* \qquad (36c)$$

The model is linearized by applying Taylor's series around the operating point and by disregarding high-order terms. This is acceptable if variations around the operating point are assumed to be small; therefore, the state-space equation of the small-signal model is obtained.

In a general sense, any function $y = f(x_1, x_2, ..., x_n)$, which has the value

$y_{ss} = f(x_{1ss}, x_{2ss}, ..., x_{nss})$ at the operating point, con be developed using Taylor's series around this point and by approximating the first-order terms:

$$y \approx y_{ss} + \left.\frac{\partial f}{\partial x_1}\right|_{ss}(x_1 - x_{1ss}) + \left.\frac{\partial f}{\partial x_2}\right|_{ss}(x_2 - x_{2ss}) + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss}(x_n - x_{nss}) \quad (37a)$$

$$y - y_{ss} \approx \left.\frac{\partial f}{\partial x_1}\right|_{ss}(x_1 - x_{1ss}) + \left.\frac{\partial f}{\partial x_2}\right|_{ss}(x_2 - x_{2ss}) + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss}(x_n - x_{nss}) \quad (37b)$$

or

$$\tilde{y} \approx \left.\frac{\partial f}{\partial x_1}\right|_{ss}\tilde{x}_1 + \left.\frac{\partial f}{\partial x_2}\right|_{ss}\tilde{x}_2 + ... + \left.\frac{\partial f}{\partial x_n}\right|_{ss}\tilde{x}_n \quad (38)$$

The variations around the operating point are indicated as: $\tilde{y} = y - y_{ss}$, $\tilde{x}_1 = x_1 - x_{1ss}$, $\tilde{x}_2 = x_2 - x_{2ss}$ and $\tilde{x}_n = x_n - x_{nss}$.

Finally, applying this linearizing method to (25) and (31):

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{DC}\end{bmatrix} = \begin{bmatrix}-\frac{R}{L} & \omega & 0\\ -\omega & -\frac{R}{L} & 0\\ -\frac{2v_{dss}}{CV_{DC}^*} & -\frac{2v_{qss}}{CV_{DC}^*} & -\frac{2(v_{dss}i_{dss}+v_{qss}i_q^*)}{CV_{DC}^{*2}}\end{bmatrix}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{DC}\end{bmatrix} + \begin{bmatrix}\frac{1}{L} & 0\\ 0 & \frac{1}{L}\\ -\frac{2v_{dss}}{CV_{DC}^*} & -\frac{2i_q^*}{CV_{DC}^*}\end{bmatrix}\begin{bmatrix}\tilde{v}_d\\ \tilde{v}_q\end{bmatrix} + \begin{bmatrix}-\frac{1}{L} & 0\\ 0 & 0\\ 0 & \frac{2}{C}\end{bmatrix}\begin{bmatrix}\tilde{E}_L\\ \tilde{i}_{DC}\end{bmatrix} \quad (39)$$

5.2 Equivalent Circuit

The equations of the steady-space representation (39) can be given as:

$$\tilde{v}_d - \tilde{E}_L = L\frac{d\tilde{i}_d}{dt} + R\tilde{i}_d - \omega L\tilde{i}_q \quad (40a)$$

$$\tilde{v}_q = L\frac{d\tilde{i}_q}{dt} + R\tilde{i}_q + \omega L\tilde{i}_d \quad \text{and} \quad (40a)$$

$$\tilde{i}_{DC} = \frac{C}{2}\frac{d\tilde{v}_{DC}}{dt} + \frac{v_{dss}}{V_{DC}^*}\tilde{i}_d + \frac{v_{qss}}{V_{DC}^*}\tilde{i}_q + \frac{i_{dss}}{V_{DC}^*}\tilde{v}_d + \frac{i_q^*}{V_{DC}^*}\tilde{v}_q - \frac{v_{dss}i_{dss} + v_{qss}i_q^*}{V_{DC}^{*2}}\tilde{v}_{DC} \quad (40c)$$

For the case of unity PF, the reference value of the reactive current component is zero ($i_q^* = 0$). Therefore, the equivalent circuit in Fig. 6 is simplified, as are its corresponding expressions.

If a PF other than zero is required, the reference value of the reactive current will be given as:

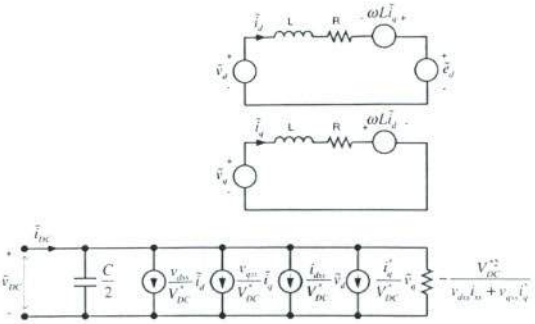

Fig. 6: Equivalent small-signal circuit.

$$i_q^* = \pm i_{dss}\sqrt{\frac{1}{PF} - 1} \quad (41)$$

In which the PF is $\cos\varphi$ when dealing with sinusoidal waveforms, and is the current phase angle in relation to the voltage phase angle. The sign in(41) will be positive for inductive PFs and negative for capacitive PFs.

6. CONCLUSION

This paper has comprehensively addressed phase models and line-to-line models of a generic n-level diode-clamped converter have been developed in this work. An average small-signal model of the three-level converter has been developed in the dq coordinates, which is applied to the design of optimal control loops. Since the modulation stage takes care of NP voltage balance the model is simplified; hence, the order of the multivariable controller can be reduced. This strategy guarantees optimal NP voltage control besides alleviating the control algorithm.

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BIOGRAPHY

Paisan Boonchiam (M'01) received the B.Eng. degree from Rajamangala Institute of Technology, Bangkok, the M.Eng. degree from Chularlongkorn University, Bangkok Thailand in 1997 and 2000 respectively.

During 1997 to 1998, he was with North Alberta Institute of Technology (NAIT), Edmonton, Alberta, Canada, and from 2001-2003, he was with the Institute of Power Electronics and Electrical Drives (ISEA), RWTH-Aachen, Aachen, Germany, as research associate.

His research areas are power system dynamics and stabiliby, power system operation, high voltage applications, power electronic, static power converter, as drives, modeling, characterization of power semiconductor devices and simulation. He is involved in more than ten research project with industrial and research council.

Mr. Boonchiam is member if Institute of Electrical and Electronic Engineering (IEEE), Institute of Engineering of Thailand (IET), and member of the European Power Electronics and Drives Association. He currently holds the lecturer of Power System Research Center, Rajamangala University of Technology Thanyaburi (RMUTT), Head of Hydro Power Plant Research Section at Center of Excellence in Sustainable Energy System (Thai-Japan), RMUTT.