New Circuit Model of Small-Signal Amplifier Developed by Using MOSFETs in Triple Darlington Configuration

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Abstract

New circuit model of MOSFET based small-signal narrow-band amplifier is proposed and qualitatively analyzed. Proposed amplifier circuit uses identical MOSFETs in Triple Darlington configuration and provides an optimum performance for the input signals swinging below 15mV. In the narrow-band performance range, the proposed amplifier produces simultaneously high voltage and current gains with low harmonic distortion. The proposed amplifier can be used to process audio range signal excursions. Variations in voltage gain as a function of frequency and different biasing resistances, temperature dependency of performance parameters, bandwidth and total harmonic distortion of the amplifiers are also perused.

Key words: Small-signal amplifiers, Darlington amplifiers, Common Source MOS amplifiers

1. INTRODUCTION

MOS transistors, in general, act as good amplifiers for radio frequency integrated circuits when operated in the saturation region (under specific characteristics) and exhibit capacity to provide high voltage, current and power gains(1,2). Simultaneously 'Common Source MOSFET' has been explored to amplify small-signals with its specific characteristic of high input impedance, low output impedance, high current gain and a voltage gain greater than unity(3,4,5,6). Numerous literatures and research papers had also explored this MOSFET configuration suitable for developing high speed switching circuits, memory segments, logic gates, buffer amplifiers, power amplifiers and trans-conductance amplifiers(1,2,3,4,5,6,7,8,9). However use of Common Source MOSFETs in Darlington's topology to develop small-signal audio range amplifiers is still to be established(5,10). In this sequence, authors developed two small-signal amplifier circuits using MOSFETs in Darlington pair and explored them as high voltage gain and wideband amplifiers respectively(5).

In the present manuscript, authors proposed a novel circuit of high voltage / high current gain audio-range small-signal amplifier by placing Common Source MOSFETs in Triple Darlington(11) configuration. Dependency of qualitative performance of the proposed amplifier on various biasing parameters, biasing supply and operational frequency is analyzed and compared with that of high voltage gain Darlington pair MOSFET amplifier(5).

2. EXPERIMENTAL CIRCUITS

The present study starts with a small-signal Darlington pair MOSFET amplifier having two N-Channel MOSFETs (IRF150) M1 and M2 in the composite unit(5). This circuit, as depicted in figure-1, is referred herein as Reference amplifier. However, the proposed amplifier, as depicted in figure-2, is obtained by adding an extra MOS transistor M3 in the circuit of reference amplifier. Assembly of MOS transistors M1, M2 and M3 in the proposed amplifier circuit (figure-2) constitutes a Triple Darlington(11) composite unit. Both the amplifiers under discussion use an extra biasing resistance R_A in respective circuits(5,10,11,12,13).

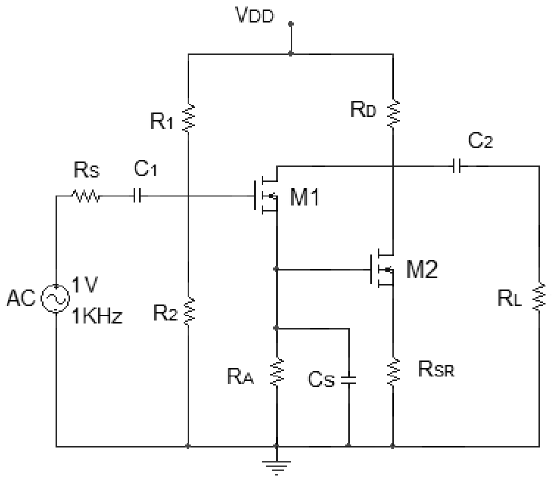


Figure-1: Darlington pair MOSFET amplifier
(Reference amplifier)

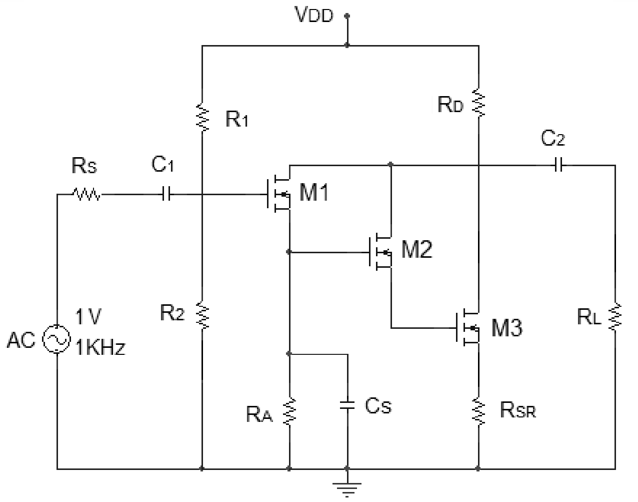


Figure-2: Triple Darlington MOSFET amplifier
(Proposed amplifier)

Table-1: Circuit components and their values

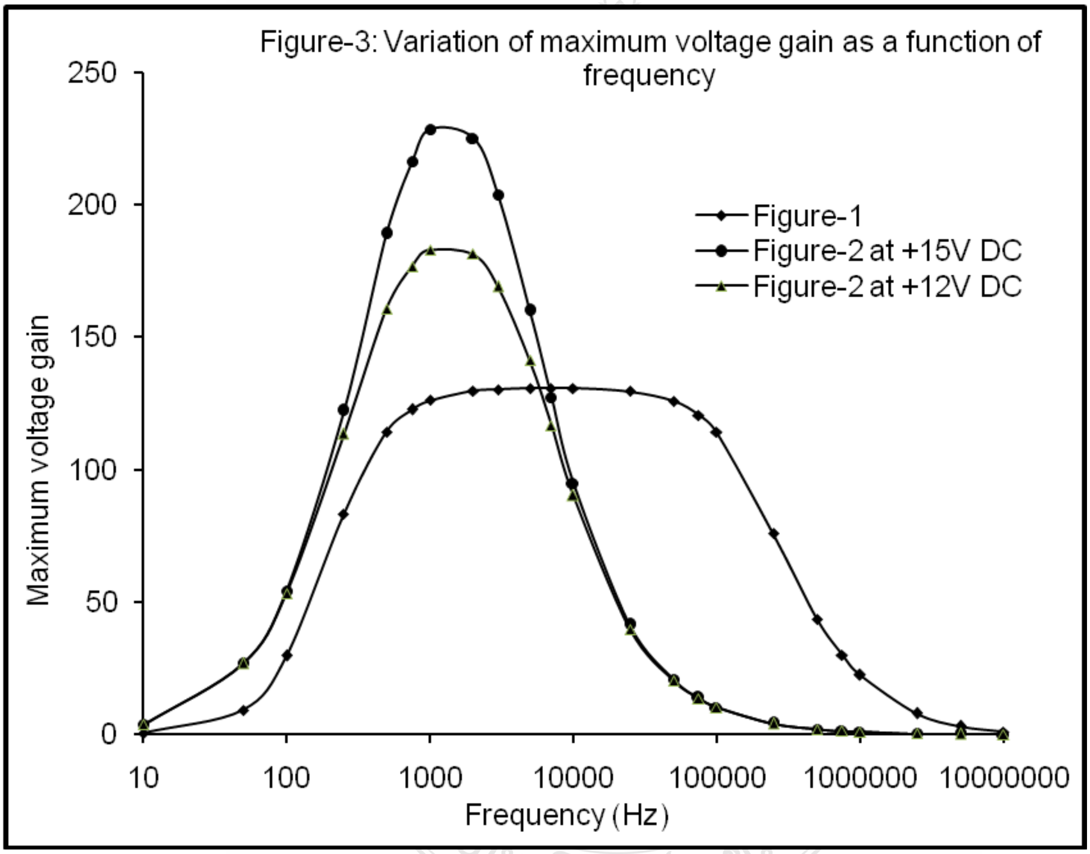
Components	Reference Amplifier (Darlington Pair MOSFET)	Proposed Amplifier (Triple Darlington MOSFET)	Proposed Amplifier (Triple Darlington MOSFET)
M_1	IRF150	IRF150	IRF150
M_2	IRF150	IRF150	IRF150
M_3	Not Available	IRF150	IRF150
R_S	250Ω	250Ω	250Ω
R_1	1.4MΩ	1.4MΩ	1.4MΩ
R_2	1MΩ	1MΩ	1MΩ
R_D	1KΩ	1KΩ	1KΩ
R_{SR}	4.5KΩ	100KΩ	100KΩ
R_A	1 KΩ	300Ω	300Ω
R_L	10KΩ	10KΩ	10KΩ
C_1	10 µF	10 µF	10 µF
C_2	0.1 µF	1 µF	1 µF
C_S	100µF	100 µF	100 µF
Biasing Supply	+15V DC	+15V DC	+12V DC
Input AC Signal range for fair output	0.1-10mV (1KHz)	0.1-2mV (at 1KHz, +15V DC)	0.1-15mV (at 1KHz, +12V DC)

The reference amplifier is biased with +15V DC supply whereas the proposed amplifier is qualitatively analyzed on two different DC biasing values i.e. at +15 Volts and +12 Volt of DC supply using potential divider network. Various biasing parameters and their values for reference and proposed amplifiers are described in Table-1.

Respective observations are made by feeding the amplifier circuits with 1V AC input signal source from which, a small and distortion less AC signal of 1mV for both the amplifiers (figure-1 and figure-2) at 1KHz frequency is drawn as input for amplification purpose. All the observations mentioned in the present manuscript are furnished through PSpice simulation software[5,10,11,12,13,14] (Student version 9.2).

3. RESULTS AND DISCUSSIONS

The amplifiers of figure-1 and 2 are found to provide fair and distortion-less results for 0.1-10mV and 0.1-2mV AC input signals respectively in 100 Hz to 100 KHz input frequency range at +15V DC biasing voltage. However, when the proposed amplifier is biased with +12V DC supply for the parameter values of Table-1, the circuit is found to provide distortion-less results for 0.1-15mV AC input signal in similar frequency range.



Variation of maximum voltage gain as a function of frequency for both the amplifiers is depicted in figure-3. It is found that the reference amplifier produces 130.6 maximum voltage gain, 7.40K maximum current gain and 178.01KHz bandwidth (with lower cut-off frequency f_L=293.134Hz and upper cut-off frequency f_H=178.305KHz). However, the proposed amplifier at +15V DC biasing supply produces 232.12 maximum voltage gain, 2.65K maximum current gain, 4.426KHz bandwidth (with f_L=379.32Hz and f_H=4.805KHz), 24.03µA peak output current and 240.28 mV peak output voltage with phase reversal in output waveform. On the other hand when the proposed amplifier is biased with +12V DC supply at the similar values of biasing parameters (Table-1), it crops 184.829 maximum voltage gain, 2.5040K maximum current gain, 5.475KHz bandwidth (with f_L=313.132Hz and f_H=5.789KHz), 18.204µA peak output current and 182.039 mV peak output voltage with phase reversal in the output waveform.

It is to be noted that the composite unit of three MOS transistors in proposed amplifier behaves as a unified Common Source MOSFET[2,3]. Therefore, when the gate voltage of this unified unit gets LOW the unit reaches in OFF mode and force output voltage to acquire HIGH status. The reverse situation exists when the gate voltage gets HIGH. This reversal switching property is responsible to produce 180^o phase difference in the output waveform[2,3,5,7,10].

Figure-3 clearly shows that the reference amplifier possesses a bandwidth of moderate range while the proposed amplifier owns narrow bandwidth at distinct DC biasing. The reason for both the circuits are having low order bandwidth is the high capacitance in composite unit of common-source MOSFET, resulting due to Miller effect(1,3,7). The virtually increased input capacitance due to Miller effect can be expressed as '$C_M=C(1+A_V)$'. Here the gate-drain capacitance is effectively multiplied by a factor $1+|A_V|$ that increases total input capacitance and results in lowering of the overall bandwidth as well as reduces its range of operation to lower frequencies.

Total Harmonic Distortion (THD) percentage is also calculated for the reference and proposed amplifiers for 10 significant harmonic terms using established formulae (3,5). For reference amplifier, THD is found to be 1.88%. However for proposed amplifier THD is found 2.84% at +15V DC biasing that reduces to 2.28% when the circuit is biased with +12V DC supply respectively. THDs for all the mentioned situations are found to be within the permissible limit of small-signal amplifiers(3). This clearly indicates that adding one more MOSFET in Darlington pair to receive proposed amplifier circuit causes about 1% increase in THD.

Variation of voltage gain, current gain and bandwidth with temperature is also measured and listed in Table-2. It is noticed here that both variety of gains gradually decreases at increasing temperature for respective amplifiers. This outcome can be associated with the positive temperature coefficient property of Drain-Source resistance(15). Perhaps Drain-Source resistance of the composite unit rises with temperature which in turn reduces the effective voltage / current gains(15). On the other hand, the bandwidth of reference amplifier reduces but that of proposed amplifier increases with rising temperature. At increasing temperature, perhaps the series combination of composite unit (having an extra MOSFET) capacitance and output coupling capacitor C_2 (with 1uF value) in the proposed amplifier circuit causes reduction in effective circuit capacitance which ultimately improves the bandwidth(1,2,15).

Table-2: Variation of Maximum Voltage gain $A_{V(MAX)}$, Maximum Current gain $A_{I(MAX)}$ and Bandwidth with temperature

Temperature (°C)	Reference Amplifier (Darlington Pair MOSFET)			Proposed Amplifier (+15V DC) (Triple Darlington MOSFET)			Proposed Amplifier (+12V DC) (Triple Darlington MOSFET)		
	$A_{V(MAX)}$	$A_{I(MAX)}$	Bandwidth (KHz)	$A_{V(MAX)}$	$A_{I(MAX)}$	Bandwidth (KHz)	$A_{V(MAX)}$	$A_{I(MAX)}$	Bandwidth (KHz)
-30	151.85	8.59K	182.53	269.26	2.74K	3.89	213.64	2.60K	4.83
-20	147.51	8.36K	181.67	261.71	2.72K	3.98	207.77	2.58K	4.97
-10	143.47	8.13K	180.71	254.65	2.70K	4.07	202.29	2.56K	5.08
0	139.69	7.92K	180.06	248.04	2.69K	4.17	197.16	2.54K	5.19
10	136.14	7.72K	178.06	241.84	2.67K	4.23	192.35	2.53K	5.30
27	130.60	7.40K	178.00	232.12	2.65K	4.47	184.82	2.50K	5.48
50	123.93	7.02K	176.44	220.41	2.62K	4.46	175.76	2.46K	5.69
80	116.41	6.58K	176.34	207.15	2.58K	4.77	165.52	2.42K	5.99
100	111.41	6.33K	176.09	199.35	2.55K	4.86	159.50	2.39K	6.16
120	107.97	6.10K	173.82	192.25	2.53K	5.03	154.03	2.37K	6.35

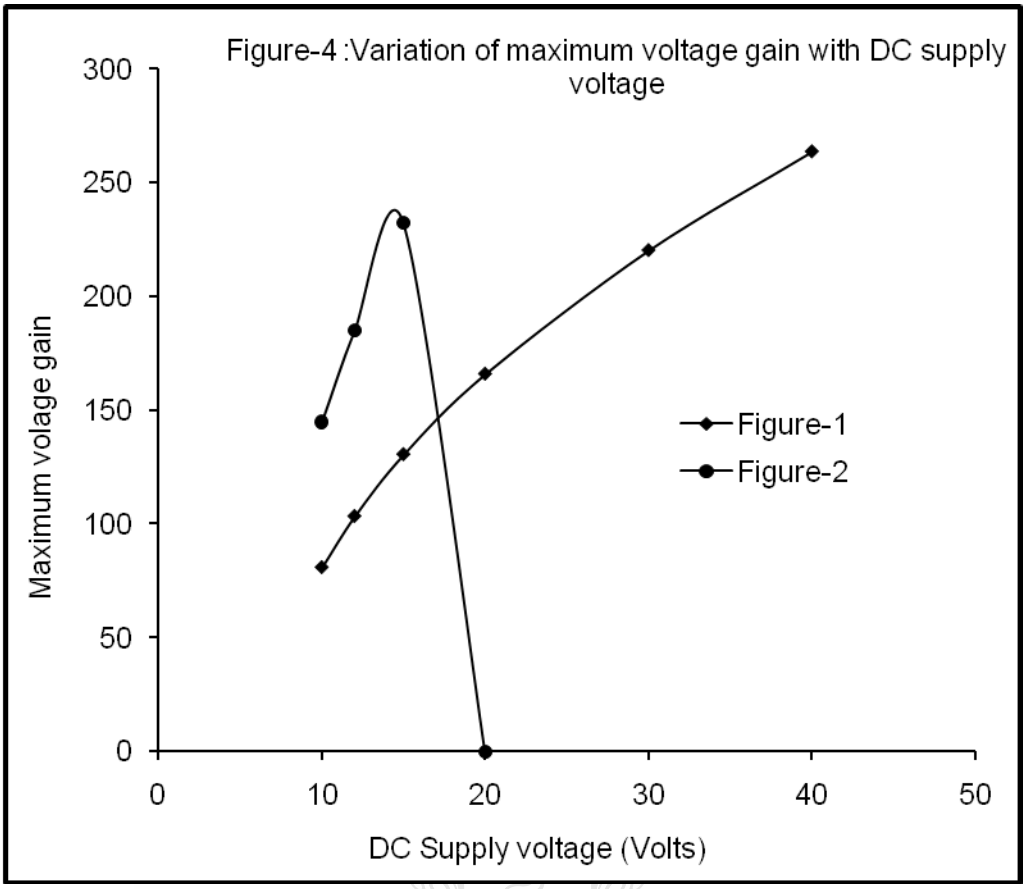


Figure-4 :Variation of maximum voltage gain with DC supply voltage
Maximum volage gain
DC Supply voltage (Volts)
Figure-1
Figure-2
300
250
200
150
100
50
0
0
10
20
30
40
50

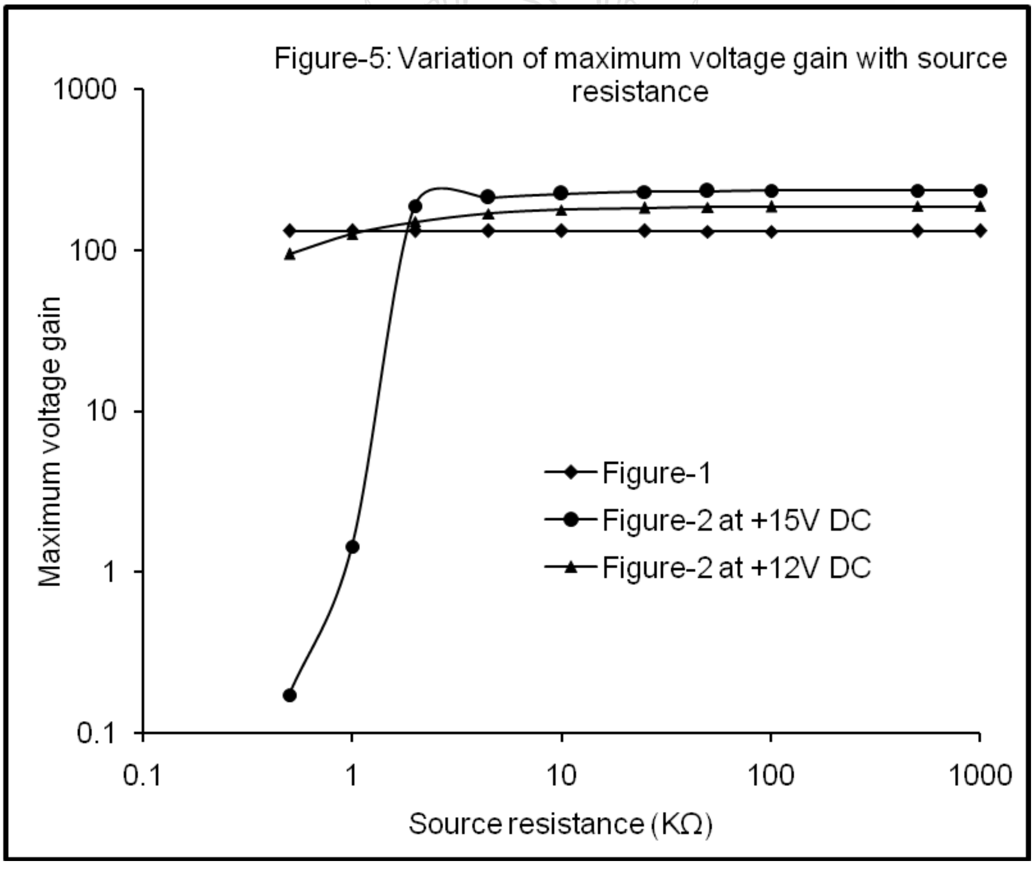
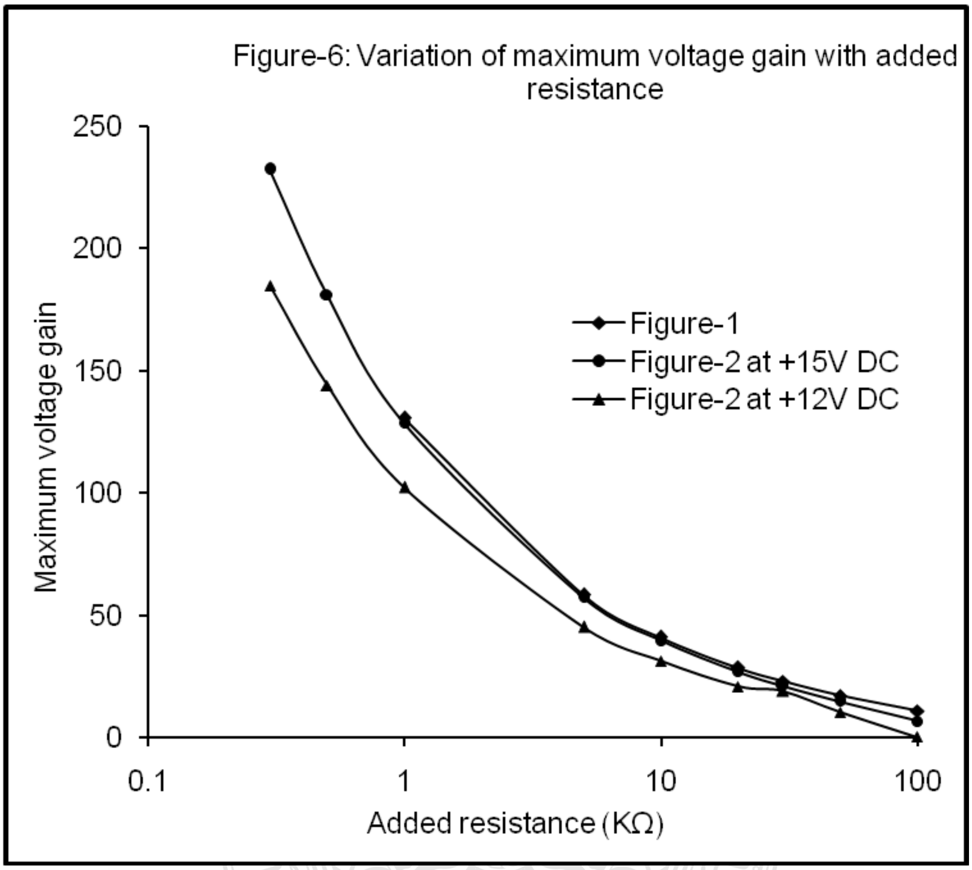


Figure-5: Variation of maximum voltage gain with source resistance
Maximum voltage gain
Source resistance (KΩ)
Figure-1
Figure-2 at +15V DC
Figure-2 at +12V DC
1000
100
10
1
0.1
0.1
1
10
100
1000

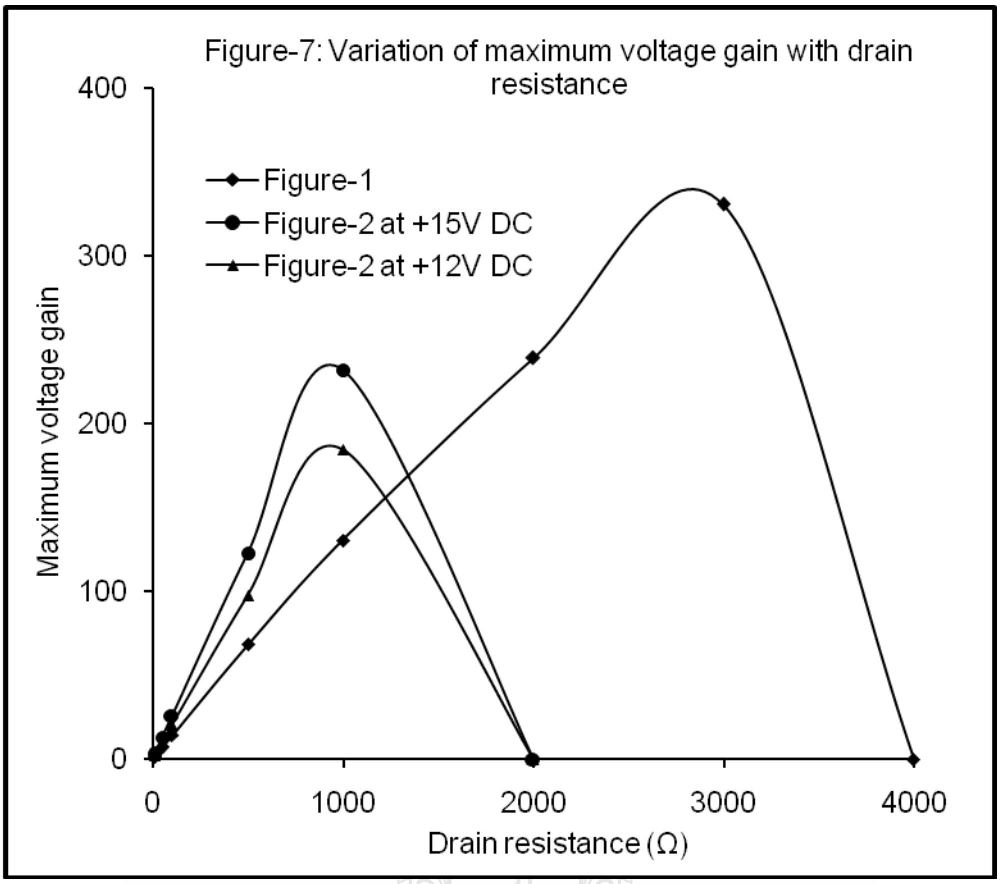
Variation of voltage gain with DC supply voltage is depicted in figure-4. Figure suggests that the voltage gain of reference amplifier rises nonlinearly at increasing values of V_{CC}(5). However it climbs up to a maximum at 15V of V_{CC} for proposed amplifier which for V_{CC}>15V decreases rapidly and reaches to a non-significant value at 20V of V_{CC}. Conclusively, the proposed amplifier provides optimal performance in 10-15V of V_{CC} whereas this range for reference amplifier is limited to 10-40V of V_{CC}.

Variation of maximum voltage gain as a function of source resistance R_{SR} is traced in figure-5. For reference amplifier and proposed amplifier (at +12V DC biasing), the voltage gain almost remains unaffected for any change in source resistance(5,10). However for proposed amplifier with +15V DC biasing, the voltage gain suddenly increases from 1.44 (at 1 KΩ) to187.38 (at 2 KΩ) and then tends to acquire a saturation tendency at higher values of R_{SR}. It is also to mention that respective amplifiers show constancy in maximum voltage gain for R_{SR}>10KΩ.



Maximum voltage gain decreases almost exponentially at increasing values of added biasing resistance R_A(5,10) for both the amplifiers under discussion. Respective graphs, as depicted in figure-6 are suggesting that in any situation the voltage gain corresponding to the added resistance R_A acquires its maxim at $R_A \leq$1KΩ. The basic role of R_A seems to provide proper biasing level to the circuits rather than contributing significantly in the gain enhancement.

Maximum voltage gain highly depends on drain resistance R_D(1,2,5,10). Its variation with R_D is depicted in figure-7. For reference amplifier, the voltage gain attains a maxim at R_D=3KΩ, thereafter decreases rapidly and produces distorted output beyond 4KΩ value of R_D. However, for proposed amplifier with +15V or +12V DC biasing, the voltage gain attains a maxim at R_D=1KΩ, then falls down rapidly and produces distorted output beyond 2KΩ.



Variation of maximum voltage gain with load resistance R_L is also observed but not shown in form of figure. Here, voltage gain gradually rises up to 100KΩ value of R_L for both the amplifiers and then tends to acquire a saturation mark. This rising and saturation tendency of the voltage gain with R_L is well in accordance of the usual behaviour of small signal amplifiers(2,5,6,10,11,12,13).

4. CONCLUSIONS

Small-signal Common Source MOSEFT amplifiers hold high current gain as its prominent feature with a voltage gain just greater than unity. However, the proposed small-signal amplifier which uses three Common Source MOSFETs in a typical Triple Darligton configuration is explored here as high voltage gain amplifier, preserving the high current gain property. In narrowband performance range (approximately 5KHz) this amplifier can effectively process small-signals ranging below 15mV. Total harmonic distortion for proposed amplifier at either of the DC supply voltage doesn't exceed beyond 2.84%, which is well within the tolerance limit of small-signal amplifiers. The proposed amplifier produces constant voltage gain at R_L>100KΩ and R_{SR}>10KΩ while shows its optimal performance at R_A<1KΩ and R_D=1KΩ in 10-15V range of DC supply voltage.

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